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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,143	07/08/2004	Satoshi Morita	103213-00091	1420

4372 7590 10/20/2005

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EXAMINER

QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/500,143

Applicant(s)

MORITA ET AL.

Examiner

Kevin Quinto

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 4, 7, 9, and 11-17 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 8 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8 July 2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 4, 7, 9, and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (United States Patent Application Publication No. US 2002/0021268 A1) in view of Yeo et al. (United States Patent Application Publication No. US 2001/0054998 A1).

4. In reference to claim 1, Yamazaki et al. (United States Patent Application Publication No. US 2002/0021268 A1, hereinafter referred to as the "Yamazaki" reference) discloses a device which meets the claim. Figures 8A and 8B of Yamazaki disclose a display device having a plurality of pixels which form a matrix-like pattern. The display device has a light-emitting element (814) that is formed in a longitudinally oblong shape in each pixel. A drive thin-film transistor (806) is formed in each pixel so that it feeds current to the light-emitting element (814) in order to make it emit light. A

control thin-film transistor (804) controls operation of the drive thin-film transistor (806).

The drive thin-film transistor is formed in a laterally oblong shape and is arranged in a length direction which is perpendicular to the length direction of the light-emitting element (814). Yamazaki does not disclose forming the drive thin-film transistor (806) and the control thin-film transistor (804) with a semiconductor layer formed of amorphous silicon. However the use of amorphous silicon to form transistors is well known in the art. Yeo et al. (United States Patent Application Publication No. US 2001/0054998 A1, hereinafter referred to as the "Yeo" reference) discloses that transistors formed of amorphous silicon have the benefits of good uniformity and a stable characteristic (p.1, paragraph 12). In view of Yeo, it would therefore be obvious to use amorphous silicon to form the drive and control thin-film transistors.

5. With regard to claim 3, the light-emitting element (814) is formed in a longitudinally oblong shape and the drive thin-film transistor (806) is formed in a laterally oblong shape. The gate signal line (803) and the source signal line (815) connecting to the control thin-film transistor (804) are arranged to form a grid-like pattern. The light-emitting element (814) is arranged in a length direction that is parallel to the source signal line (815). The drive thin-film transistor (806) is arranged in a length direction that is parallel to the gate signal line (803).

6. In reference to claim 4, the drive thin-film transistor (806) has a channel region that is formed in an elongate shape and is arranged such that the length direction of the channel region is parallel to the gate signal line (803).

7. With regard to claim 7, each row of the matrix-like pattern has a gate signal line (803) that is connected to the gate electrodes (804a, 804b) of all the control thin-film transistors in pixels located in a row. A power feed line (816) from which current is fed via the drive thin-film transistors (806) to the light-emitting elements (814) in the row. Each column of the matrix-like pattern has a source signal line (815) that is connected to the source electrodes of all of the control thin-film transistors (804) in pixels located in the column and crosses the gate signal line (803). Within the area surrounded by the gate signal lines (803) and the source signal lines (815), the light emitting element (814), the drive thin-film transistor (806), the power feed line (816), and the control thin-film transistor (804) are arranged in this order along the source signal line (815) as seen in a plan view.

8. With regard to claim 9, Yamazaki makes it clear that the display device of figures 8A and 8B may have the physical configurations shown in figures 1-6 (p. 10, paragraph 166). The display device of Yamazaki comprises light-emitting elements that emit light of different colors (p. 3, paragraphs 61-69). A plurality of power feed lines (816) is formed to correspond to light of the different colors. The plurality of power feed lines (816) is arranged between the drive thin-film transistor (806) and the control thin-film transistor (804). The light-emitting elements (814) are fed with a current from the corresponding power feed lines (816).

9. In reference to claim 11, Yamazaki makes it clear that the display device of figures 8A and 8B may have the physical configurations shown in figures 1-6 (p. 10, paragraph 166). Figures 1-6 of Yamazaki disclose the use of a bank layer (390) which

is arranged around the light-emitting element (389, 391, 392, 393). The bank layer (390) overlaps the drive thin-film transistor (504). A cut is formed in the bank layer (390) between the light emitting element (389, 391, 392, 393) and the drive thin-film transistor (504). Yamazaki uses a cathode (392) made of aluminum at a thickness of 80 to 200 nm (p. 9, paragraph 138) that is formed on the bank layer (390) at least in a portion near the cut. Yamazaki et al. (United States Patent Application Publication No. US 2005/0007331 A1, hereinafter referred to as the "Yamazaki 331" reference) discloses that aluminum at a thickness 100 to 300 nm can be used as a light shielding film (p.12, paragraph 253). Therefore the cathode (392) of Yamazaki may act as a light-shielding film.

10. In reference to claim 12, Yamazaki makes it clear that the display device of figures 8A and 8B may have the physical configurations shown in figures 1-6 (p. 10, paragraph 166). Figures 1-6 of Yamazaki disclose the use of a bank layer (390) which is arranged around the light-emitting element (389, 391, 392, 393). The bank layer (390) overlaps the control thin-film transistor (503). A cut is formed in the bank layer (390) between the light emitting element (389, 391, 392, 393) and the control thin-film transistor (503) formed in a next pixel. Yamazaki uses a cathode (392) made of aluminum at a thickness of 80 to 200 nm (p. 9, paragraph 138) that is formed on the bank layer (390) at least in a portion near the cut. Yamazaki 331 discloses that aluminum at a thickness 100 to 300 nm can be used as a light shielding film (p.12, paragraph 253). Therefore the cathode (392) of Yamazaki may act as a light-shielding film.

11. In reference to claim 13, Yamazaki makes it clear that the display device of figures 8A and 8B may have the physical configurations shown in figures 1-6 (p. 10, paragraph 166). Figures 1-6 of Yamazaki disclose the use of a bank layer (390) which is arranged around the light-emitting element (389, 391, 392, 393). The bank layer (390) covers the drive thin-film transistor (504) and control thin-film transistor (503). The bank layer (390) has edges located between the drive thin-film transistor (504) and the control thin-film transistor (503) and the light-emitting element (389, 391, 392, 393). Yamazaki uses a cathode (392) made of aluminum at a thickness of 80 to 200 nm (p. 9, paragraph 138) that is formed on the bank layer (390). Yamazaki 331 discloses that aluminum at a thickness 100 to 300 nm can be used as a light shielding film (p.12, paragraph 253). Therefore the cathode (392) of Yamazaki may act as a light-shielding film.

12. With regard to claim 14, Yamazaki makes it clear that the display device of figures 8A and 8B may have the physical configurations shown in figures 1-6 (p. 10, paragraph 166). The display device shown in figures 1-6 has a pixel electrode (389) that is arranged below a light-emitting layer (391) of the light-emitting element and is connected to the drive thin-film transistor (504). A common electrode (392) is arranged to face the pixel electrode (389) with the light-emitting layer (391) interposed between them while covering the bank layer (390). Yamazaki uses a common electrode (392) made of aluminum at a thickness of 80 to 200 nm (p. 9, paragraph 138). Yamazaki 331 discloses that aluminum at a thickness 100 to 300 nm can be used as a light shielding

film (p.12, paragraph 253). Therefore the common electrode (392) of Yamazaki may act as a light-shielding film.

13. In reference to claims 15 and 16, Yamazaki discloses the use of n-channel and p-channel type thin-film transistors for the drive thin-film transistor and the control thin-film transistor (p. 9, paragraphs 107-108).

14. With regard to claim 17, Yamazaki makes it clear that the light-emitting element is of an organic electroluminescence type (p. 1, paragraph 2 and p. 2, paragraph 21).

Allowable Subject Matter

15. Claims 5, 6, 8, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a display device with thin-film transistors with the laterally oblong drive thin-film transistor and the surrounding electrode shapes as disclosed by the applicant.

Conclusion

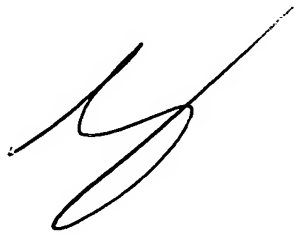
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

A handwritten signature in black ink, appearing to be 'Nathan J. Flynn', written in a cursive style.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800